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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,083	02/27/2004	Bang-Chein Ho	252016-1710	7532

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EXAMINER	
LE, DUNG ANH	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

A

Office Action Summary	Application No.	Applicant(s)	
	10/789,083	HO ET AL.	
	Examiner	Art Unit	
	DUNG A. LE	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) ~~1~~ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

The oath/declaration filed on 2/27/2004 is acceptable.

Election/Restriction

Application's election **without traverse** of Group II (Claims 1-15) drawn to process of making a semiconductor device is acknowledged for prosecution in the subject application . Applicants have the right to file a divisional, continuation or continuation-in-part application covering the subject matter of the non-elected claims 16-23.

Information Disclosure Statement

This office acknowledges of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 2/27/2004 has/have been considered and made of record. The references cited on the PTOL 1449 form have been considered.

Drawings

The drawings are objected to for the following reasons.

Figures 1E-1H should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction

or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1- 7 are rejected under 35 USC 102 (b) as being anticipated by Okada et al. (6,514,860 B1).

Okada teaches a method of forming a dual damascene interconnect (3A-3M and related texts) in an integrated circuit comprising:

providing a substrate 110 (col 7, lines 20-21) having a first etched region 116 therein;

filling said first etched region 116 with a protective layer 148 (col 9, line15-20); coating said protective layer 148 with a resist layer 150;

patterning said resist layer 150 and said protective layer 148 to define an opening encompassing said first etched opening wherein said protective layer is recessed within said first etched opening (fig. 3H and related texts);

thereafter forming a second etched region 146 encompassing a top portion of said first etched region 116;

thereafter removing said resist layer 150 and said protective layer 148; and

thereafter filling said first and second etched regions 116/146 with a conductive material 122 to complete formation of said interconnect (figs. 3L-3M and related texts).

Regarding claim 2, wherein said protective material is a bottom antireflective coating (BARC) material (col 9, lines 15-20).

Regarding claim 3, wherein said BARC material has the following properties: it absorbs light at a wavelength (col 9, lines 20-25) used to expose said resist; it completely fills said first etched region; and it can be partially removed by a developer used to remove said resist (figs .3G- 3H and related texts).

Regarding claim 4, wherein said BARC material comprises polyimide or organic type ARC material (col 9, line 24).

Regarding claim 5, wherein said first etched region forms a via hole 116 and wherein said second etched region forms a trench 146 and wherein said via hole 116 and said trench together form a dual damascene opening (figs. 3I- 3J and related texts).

Regarding claim 6, wherein the said protective layer 148 recessed within said first etched region 116 has a height of between about 50% and 95% of a height of said first etched region (fig. 3G).

Regarding claim 7, wherein said first and second etched region are etched through an insulating layer 142/114 comprising silicon dioxide or low dielectric constant dielectric materials (col 8, line 26 and col 7, line 65).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 7 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Okada in view of Lee et al. (6861347 B2).

Okada disclosed the claimed invention as applied to claim 1 including a hard mask layer 117 overlying said insulating layer 142/114 prior to forming said first etched region except for hard mask layer comprises silicon nitride as cited in current claim.

Lee et al. teach the hard mask layer 308 comprises silicon nitride overlying said insulating layer prior to forming said first etched region (fig. 13, lines 50-55).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the hard mask layer comprises silicon nitride overlying said insulating layer prior to forming said first etched region in Okada 's method, in order to simplify the process of creating the via hole because it has a low etching selectivity to insulating layer.

Set of claims 9-15

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 9- 14 are rejected under 35 USC 102 (b) as being anticipated by Okada et al. (6,514,860 B1).

Okada teach a method of forming a dual damascene (figs. 3A-3M and related texts) interconnect in an integrated circuit comprising:

providing a substrate 110 (col 7, line 21) having a first etched region 116 11therein;

filling said first etched region with a bottom antireflective coating (BARC)

layer 148 (col 9, lines 15-20);

coating said BARC layer with a resist layer 150;

patterning said resist layer and said BARC layer to define an opening encompassing said first etched opening wherein said BARC layer is recessed within said first etched opening (3G-3H and related texts);

thereafter forming a second etched region 146 encompassing a top portion of said first etched region 116;

thereafter removing said resist layer and said BARC layer (figs. 3H-3J and related texts) ; and

thereafter filling said first and second etched regions with a conductive material 122 to complete formation of said interconnect (fig. 3M and related texts).

Regarding claim 10, wherein said BARC material has the following properties: it absorbs light at a wavelength used to expose said resist; it completely fills said first etched region; and it can be partially removed by a developer used to remove said resist (col 9, lines 15-25, fig. 3G-3H and related texts).

Regarding claim 11, wherein said BARC material comprises polyimide or organic type ARC material (col 9, lines 15-20).

Regarding claim 12, wherein said first etched region forms a via hole 116 and wherein said second etched region forms a trench 146 and wherein said via hole and said trench together form a dual damascene opening.

Regarding claim 13, wherein the said BARC layer 148 recessed within said first etched region has a height of between about 50% and 95% of a height of said first etched region (figs 3G-3H and related texts).

Regarding claim 14, wherein said first and second etched region are etched through an insulating layer 142/114 comprising silicon dioxide or low dielectric constant dielectric materials (col 8, line 26 and col 7, line 65).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention

was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 15 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Okada in view of Lee et al. (6861347 B2).

Okada disclosed the claimed invention as applied to claim 9 including a hard mask layer 117 overlying said insulating layer 142/114 prior to forming said first etched region except for hard mask layer comprises silicon nitride as cited in current claim.

Lee et al. teach the hard mask layer 308 comprises silicon nitride overlying said insulating layer prior to forming said first etched region (fig. 13, lines 50-55).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the hard mask layer comprises silicon nitride overlying said insulating layer prior to forming said first etched region in Okada 's method, in order to simplify the process of creating the via hole because it has a low etching selectivity to insulating layer.

When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung A. Le whose telephone number is (571) 272-1784. The examiner can normally be reached on Monday-Tuesday and Thursday 6:00am- 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The central fax phone numbers for the organization where this application or proceeding is assigned are (571)272-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DL

DUNG LE
PRIMARY EXAMINER